## IN THE UNITED SPATES PATENT & TRADEMARK OFFICE

Applicant:

LIU et al.

Docket No:

16405-0013

Serial No:

09/827,056

Group Art Unit:

2811

Filing Date:

: April 3, 2001

Examiner:

Tran, T.F.

For:

METHOD OF FABRICATING HIGH-COUPLING RATIO SPLIT GATE

FLASH MEMORY CELL ARRAY

Commissioner of Patents and Trademarks Washington, D.C. 20231

## **RESPONSE**

Sir:

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Responsive to the Office Action mailed May 9, 2002, please amend the above identified application as follows.

## **IN THE CLAIMS**

Please amend the claims as follows:

1. (Once amended) A method of fabricating a flash memory device including an array of split gate cells, comprising the steps of:

providing a silicon substrate having a top surface;

forming a common source region in an area of said top surface for each said cell;

implanting ions into predefined areas on opposite sides of each said common source region;

forming pair of floating gates associated with each said cell, each said floating gate having a substantial portion thereof overlying one of said predefined areas;

forming select gates each having a first extremity extending over at least a portion of one of said floating gates; and

forming a pair of drain regions associated with each said cell, each said drain region being positioned proximate a second extremity of one of said select gates;

whereby said step of implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell.